22 NOV 95 10:47:52 U.S. Patent & Trademark Office P0002

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  *                WELCOME  TO  THE                            *
  *         U. S.  PATENT  TEXT  FILE                         *
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=> s 395/?/ccls
L1        26522 395/?/CCLS

=> s l1 and (clock? (5a) in (5a) interface?)/ab
          16405 CLOCK?/AB
         225631 IN/AB
          15960 INTERFACE?/AB
              2 (CLOCK? (5A) IN (5A) INTERFACE?)/AB
L2            0 L1 AND (CLOCK? (5A) IN (5A) INTERFACE?)/AB

=> s clock? (5a) in (5a) interface?
         238405 CLOCK?
        1809332 IN
           165798 INTERFACE?
L3          110 CLOCK? (5A) IN (5A) INTERFACE?

=> s l3 and l1
L4           46 L3 AND L1

=> s l4 and microprocessor?/ab
          8122 MICROPROCESSOR?/AB
L5           2 L4 AND MICROPROCESSOR?/AB

=> d l5 kwic 1-2

US PAT NO:      5,255,377 [IMAGE AVAILABLE]              L5: 1 of 2
US-CL-CURRENT: 395/412; 364/242.7, 254.3, 263.1, DIG.1

ABSTRACT:
An arrangement in a microprocessor having both a segmentation addressing
scheme and a page mode addressing scheme which arrangement reviews requests
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US PAT NO: 5,408,641 [IMAGE AVAILABLE] L4: 10 of 46

SUMMARY:

BSUM(9)

In . . . of various memory units at different speeds with a single CPU, separate clocks with a fixed phase relationship are required. In addition, this arrangement requires a clock distribution cable and interface arrangement between the CPU and its associated memory units, just as is the case with synchronous systems. The elimination of. . .

US PAT NO: 5,402,526 [IMAGE AVAILABLE] L4: 11 of 46
US-CL-CURRENT: 395/53, 50

DETDESC:

DETD(391)

The . . . receives it from the I/O interfaces (discussed in the Interface Requirements section), or from local sources (knowledge sources, the user interface, or the system clock). In any case, once the data is received, it is written on the blackboard, if appropriate, and tested for event generation.. . .

US PAT NO: 5,398,304 [IMAGE AVAILABLE] L4: 12 of 46
US-CL-CURRENT: 395/53, 50

DETDESC:

DETD(392)

The . . . receives it from the I/O interfaces (discussed in the Interface Requirements section), or from local sources (knowledge sources, the user interface, or the system clock). In any case, once the data is received, it is written on the blackboard, if appropriate, and tested for event generation.. . .

US PAT NO: 5,388,265 [IMAGE AVAILABLE] L4: 13 of 46
US-CL-CURRENT: 395/750; 364/232.8, 273, 273.1, 707, DIG.1; 371/22.5; 395/550

DETDESC:

DETD(21)

FIG. . . . 406-413, floppy disk drive (FDD)interface 402, serial data interface 403, microcode and control logic 404 and power down logic and clock generator 405. In the currently preferred embodiment, bus interface logic 401 provides an interface between FDC 400 an the digital computer by receiving a chip select CS signal, a. . .

US PAT NO: 5,369,735 [IMAGE AVAILABLE] L4: 14 of 46
US-CL-CURRENT: 395/123; 348/580; 395/125

DETDESC:

DETD(70)

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US PAT NO: 5,255,377 [IMAGE AVAILABLE] L4: 23 of 46
US-CL-CURRENT: 395/412; 364/242.7, 254.3, 263.1, DIG.1

DETDESC:

DETD(21)

The timing diagram of FIG. 2 illustrates the basic flow of information through the interface. In phase one of clock cycle 1, the S unit 10 initiates a request for the linear address bus by asserting Sreq; the signal is. . .

US PAT NO: 5,247,650 [IMAGE AVAILABLE] L4: 24 of 46
US-CL-CURRENT: 395/500; 364/221, 221.9, 222, 271.9, DIG.1

DETDESC:

DETD(41)

Connected to each communications portion 220 is a synchornization portion 222, interface service portion 224, and clock 226. In simulation systems, such as 206, containing multiple devices 218, a multi-device synchronization and routing unit 228 is also placed having. . .

US PAT NO: 5,243,699 [IMAGE AVAILABLE] L4: 25 of 46
US-CL-CURRENT: 395/858; 364/DIG.1; 395/800

DETDESC:

DETD(128)

CLK. Parallel interface clock input. This input furnishes the clocks for the parallel interface circuitry. In keeping with normal convention, the 0-to-1 transition of this clock is the active edge. CLK is allowed to be completely. . .

US PAT NO: 5,235,698 [IMAGE AVAILABLE] L4: 26 of 46
US-CL-CURRENT: 395/550

DETDESC:

DETD(7)

FIG. . . . standard interface, the phase of the interface clock is adjusted at time tp so that from time tp onwards, the interface clock and the standard clock are not in phase. In addition, before the CPU completes is access to the standard interface, or at time tQ, the interface clock would ordinarily change from "1" to "0". In order for the interface clock and CPU clock to fall from "1" to "0" at the same time, the interface clock signal is forced to. . .

US PAT NO: 5,228,134 [IMAGE AVAILABLE] L4: 27 of 46
US-CL-CURRENT: 395/465; 364/238.6, 239.51, 243.4, 926.1, 926.9, 926.91, 926.92, 927.8, 927.92, 927.93, 927.95, 940, 940.81, 942, 948.34, 950, 950.1, 950.3, 959.1, 964, 964.2, DIG.1, DIG.2; 395/469, 470, 473

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US PAT NO: 4,777,618 [IMAGE AVAILABLE] L4: 34 of 46
US-CL-CURRENT: 395/500; 364/431.04, 920, 921, 921.3, 921.8, 926, 926.9, 926.91, 927.2, 927.4, 927.92, 927.99, 928, 928.5, 933.8, 934, 934.1, 937.01, 940, 940.1, 940.2, 941, 941.2, 941.5, 942.7, 947, 947.2, 947.3, 950, 950.3, 950.5, 950.61, 952, 952.1, DIG.2

DETDESC:

DETD(62)

In the first embodiment, the clock 34A in the ECU panel interface 34 for adding the time information to the internal information is formed independently of each of the clock 38E in. . .

DETDESC:

DETD(68)

In this third embodiment, the clock of the ECU panel interface 34 is dispensed with and the ECU panel interface 34 is controlled in external synchronism by the external clock CLK2. . .

US PAT NO: 4,760,406 [IMAGE AVAILABLE] L4: 35 of 46
US-CL-CURRENT: 346/33R; 340/825.14; 347/247; 358/296; 364/DIG.2; 395/250

SUMMARY:

BSUM(8)

In . . . such RAM, provided in the host system and then the data is transferred to the printer in accordance with the clock signal supplied from the printer. In the preferred embodiment, the printer interface circuit includes an expansion circuit comprised of a frequency divider, so that expansion circuit converts the time period of the. . .

US PAT NO: 4,695,952 [IMAGE AVAILABLE] L4: 36 of 46
US-CL-CURRENT: 395/308; 364/232.9, 240, 240.2, 240.5, 240.7, 240.8, 240.9, 241.9, 244, 244.8, 259, 259.9, 284, 284.3, DIG.1

DETDESC:

DETD(74)

A . . . DMA configurations. A MEMORY ACCESS CLOCK signal on a line 716 has an active low synchronizing output used to generate interface reads or writes to memory. In DMA mode, the MEMORY ACCESS CLOCK signal is more suitably called a DMA ACKNOWLEDGE. The host system uses the DMA REQUEST line to determine that the. . . via the DMA ACKNOWLEDGE (MEMORY ACCESS CLOCK) to the control and error logic 436 that the memory is available for interface access. In transparent mode, the MEMORY ACCESS CLOCK signal indicates bus cycles and the interface uses it automatically to read or write memory if the host processor is. . .

US PAT NO: 4,691,294 [IMAGE AVAILABLE] L4: 37 of 46
US-CL-CURRENT: 395/550; 364/919, 920.7, 927.92, 937, 940.81, 942.03, DIG.2; 370/103; 380/48
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US PAT NO: 4,192,004 [IMAGE AVAILABLE] L4: 44 of 46

DETD(5)

As . . . and a display matrix 20. Also shown is a video camera 22 focused on a scanned field 24, a camera interface 26, and a clock pulse generator 28. In the illustrative embodiment, the camera produces a binary image matrix having one hundred and twenty-eight elements on each side, i.e.,. . .

US PAT NO: 3,980,993 [IMAGE AVAILABLE] L4: 45 of 46
US-CL-CURRENT: 395/550; 364/232.8, 239, 239.1, 270, 270.3, DIG.1

SUMMARY:

BSUM(13)

More . . . a pair of high-speed two-phase clocks, and the low-speed circuitry is to be clocked by a pair of low-speed two-phase clocks. In such an arrangement the interface circuitry further includes a third sampling device, a third storage device connected to receive the output thereof, a fourth sampling. . .

US PAT NO: 3,909,818 [IMAGE AVAILABLE] L4: 46 of 46
US-CL-CURRENT: 395/150; 345/124; 395/153

DETDESC:

DETD(30)

FIG. . . . a dial-up port 160; a newsline interface 162; select logic 164; a priority encoder 166; output display logic 168; a clock and thermometer interface 170; and In/Out buffers 171.

DETDESC:

DETD(37)

The . . . UP and DN from the temperature sensor 108 and applies an instruction signal designated CLEAR to the temperature sensor 108. In addition, the clock and thermometer interface receives a 1Hz signal from the sync frequency synthesizer 110 and applies an instruction signal designated COTCHA to the temperature. . .

=>

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US005235698A

United States Patent [19]

Lan

[11] Patent Number: 5,235,698

[45] Date of Patent: Aug. 10, 1993

[54] BUS INTERFACE SYNCHRONIZATION CONTROL SYSTEM

[75] Inventor: Ray-Yuan Lan, Taipei, Taiwan

[73] Assignee: Acer Incorporated, Taipei, Taiwan

[21] Appl. No.: 405,986

[22] Filed: Sep. 12, 1989

[51] Int. Cl.[5] G06F 1/12

[52] U.S. Cl. 395/550

[58] Field of Search 364/200, 900; 395/550

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Primary Examiner—Eugene R. LaRoche
Assistant Examiner—Michael C. Kessell
Attorney, Agent, or Firm—Kenneth M. Kaslow

[57] ABSTRACT

The interface control system of this invention renders a high speed CPU compatible with low speed expansion devices such as expansion interfaces. The system causes the CPU clock signal to be in phase with the interface clock signal at the end of the last cycle of an interface cycle. At the end of the interface cycle, the system selects between a positive high speed and a negative high speed clock to be the CPU clock signal applied to the CPU.

13 Claims, 16 Drawing Sheets